REMARKS

Claims 1-21 are pending in the present application.

This Amendment is in response to the Office Action mailed July 18, 2001. In the Office Action, the Examiner rejected claims 1, 4-8, 11-15 and 18-21 under 35 U.S.C. § 102(e) and claims 2-3, 9-10 and 16-17 under 35 U.S.C. § 103(a). Reconsideration in light of the remarks made herein is respectfully requested.

I. REJECTIONS UNDER 35 U.S.C. § 102(b) AND § 103(a)

In the Office Action, the Examiner rejected claims 1, 4-8 and 11-15 and 18-21 under 35 U.S.C. § 102(e) as being unpatentable over U.S. Patent No. 5,802,569 issued to Genduso et al. ("Genduso") . The Examiner rejected claims 2-3, 9-10 and 16-17 under 35 U.S.C. § 103(a) as being unpatentable over Genduso in view of U.S. Patent No. 5,309,451 issued to Noya ("Noya"). Applicants respectfully traverse the rejections for the following reasons.

Applicants re-iterate the arguments set forth in the previously filed Response to the Office Action. In particular, Applicants maintain that Genduso and Noya, taken alone or in any combination, do not disclose, suggest, or render obvious prefetching data to a cache queue.

In the Office Action, the Examiner stated that "a queue sometimes can be FIFO, sometimes it is not (computer dictionary, third edition), a queue can be a data structure which removal is based on factors other than order of insertion. Also, nothing in the claim requires the cache queue to be FIFO." This argument is flawed in several aspects.

First, the definition in the Microsoft Press Computer Dictionary is mainly for software. A person skilled in the art of hardware design would understand that a hardware queue is a first-in-first-out device. Applicants are enclosing in Appendix A application note titled "Understanding the IDT7201/7202 FIFO" ("Application Note") from Integrated Device Technology. The relevant excerpt is as follows:

> "...Queues are a linear organization of groups of latches. Access to the linear string is restricted to either end. While RAMs allow for random access of any data in the array at any point in time, they require address inputs. Queues on the other hand, don't have an address thus avoiding the address operation and storage overhead. Queues can be divided into two categories: FIFOs and LIFOs" (Application Note, page 9-1).

Second, although the claim does not explicitly state the FIFO nature of the queue, it is well known that the claims must be "given the broadest reasonable interpretation consistent with

the specification." MPEP 2111 (Emphasis added). The "PTO applies to verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in applicant's specification." In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Claims should be interpreted consistently with the specification, which provides content for the proper construction of the claims because it explains the nature of the patentee's invention. See Renishaw, 158 F.3d 1250. The specification as a whole must be considered in determining what the ... Patent protects. See Hyatt v. Boone, 146 F.3d 1348, 1353 (Fed. Cir. 1998). Claims must be read in the context of the specification and prosecution history, as a person skilled in the art would read them. Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996); Bell Communications Research, Inc. v. Vitalink Communications Corp., 55 F.3d 615, 619

Here, the specification provides full support for the FIFO nature of the queue. Figures 3A, 3B, 4A, and 4B show the data delivery and purging to follow the first-in-first-out order (e.g., 0-1a, 0-1b,0-1c,...) as explained in the Specification on page 11 (lines 4-23) and pages 12-15.

Third, even if the claim only recites "queue" and not "FIFO" explicitly, "queue" is not defined as a random access memory (RAM) in the Computer Dictionary by Microsoft Press. This is understandable because if the queue operates the same way as a RAM, then there is no need to have different names. Therefore, the claims as written does not written on the cited prior art references, which use RAM.

Therefore, Applicants believe that independent claims 1, 8 and 15 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicant(s) respectfully request(s) the rejections under 35 U.S.C. § 102(e) and 103(a)be withdrawn.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

There has been no change to the claims.

CONCLUSION

In view of the amendments and remarks made above, it is respectfully submitted that the pending claims are in condition for allowance, and such action is respectfully solicited.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: September 28, 2001

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: September 28, 2001.

Barbara Hayashi 9/28/01
Date

APPENDIX A

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1990-91
SPECIALIZED MEMORIES
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Integrated Device Technology, Inc.

UNDERSTANDING THE IDT7201/7202 FIFO

APPLICATION NOTE AN-01

by Michael J. Miller

INTRODUCTION

This article discusses several different types of FIFO queues, their implementation, their performance and their use. Data, or information in computers, is processed as words or bytes in a predominantly serial fashion. There are producers and consumers of information that are connected by busses. Often there is a mismatch in the rate at which data is produced and the rate at which it can be accepted. The data is therefore buffered in serial lists until it can be used. The serial lists are stored in memory and require overhead to maintain them. These First-In-First-Out (FIFO) structures can be implemented at many levels from all software to all hardware. The software implementations are often the most flexible but yield the lowest performance. The hardware implementations, while less flexible, give the highest performance.

QUEUES

The elements of any computer or controller can be divided into three categories in relation to information: transformation, storage and transfer. Logic gates transform and combine information, memory elements store information and wires transfer information between the other elements.

Memory can be viewed as an element which transfers information with respect to time. The simplest of memory elements are latches and registers. RAMs are dense arrays of latches. While RAMs allow for dense information storage, they require an address to access individual pieces of information in the array. Therefore, addresses (information) must be generated and stored in order to access the desired information. The addresses are stored in programs and data structures such as linked lists.

Queues are a special organization of dense arrays of latches. Queues are a linear organization of groups of latches. Access to the linear string is restricted to either end. While RAMs allow for random access of any data in the array at any point in time, they require address inputs. Queues on the other hand, don't have an address thus avoiding the address generation and storage overhead. Queues can be divided into two categories: FIFOs and LIFOs.

Queues can be observed in the world about us. FIFO is an acronym for "First-In-First-Out". They can be observed in a bank line-up where customers enter at the end of a line, and after some wait, are serviced at the other end. The FIFO queue provides a mechanism by which customers which arrive at an erratic rate can wait until a teller can accommodate them.

LIFO is an acronym for "Last-In-First-Out". We can observe this phenomenon in the work place. As a person is working at a desk, interrupts occur. A higher priority interrupt such as a phone call or a request from people higher in management will cause the person to drop the work on the desk and start a new task. When the higher priority task is accomplished, the interrupted task on the desk is resumed. Depending on how many interrupts of sequentially higher priority tasks come in during the day, the stack of tasks on the desk grows. Another time honored example is the stacks of trays at the cafeteria. As trays are washed they are placed on a spring loaded elevator which sinks down to accommodate the new trays. When new customers enter the food line, trays are removed from the stack.

As can be seen in the above examples, queues are used to buffer between the flows of consumers and distributors of services. Groups of computing elements can be divided into consumers and producers of information with rates that must be matched. For example, a rotating Winchester disk is a source of information that must be serviced at a rate that may not be easily matched by the CPU which is consuming the information through the use of a data bus.

SIMPLE FIFO

The implementation of FIFOs is varied and presents many trade-offs. The simplest design treats the FIFO as a fixed number of memory elements in a linear array. When data is

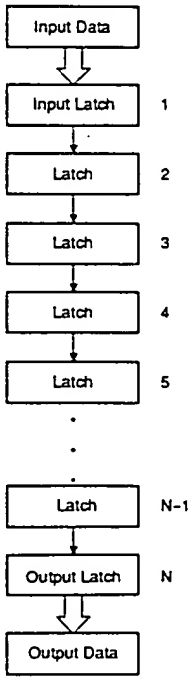

Figure 1. Hardware Implementation of a Fixed Length FIFO